2. (TWICE AMENDED) The circuit according to claim 12, wherein said [plurality of output clocks] one or more clock signals are individually programmable to oscillate at a different one of said plurality of frequencies.

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Sub D1

3. (AMENDED) The circuit according to claim 12, wherein said [second] programmable logic circuit comprises a product term array [comprises a phase lock loop (PLL)].

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4. (TWICE AMENDED) The circuit according to claim 12, wherein said [plurality of output clocks are accessible through one or more input/output pins] programmable logic circuit comprises a look-up table.

Sub C1

5. (TWICE AMENDED) The circuit according to claim 12, wherein said one or more clock signals each [output clocks] have an impedance that [may] can be adjusted [in response to said one or more programming inputs] to match [the] an external impedance [of an external device].

6. (TWICE AMENDED) The circuit according to claim 12, wherein said [output] plurality of frequencies can be programmed after fabrication and installation of said [programmable] device.

B

7. (TWICE AMENDED) The circuit according to claim 12, wherein said reference clock frequency is selected from one or more reference clock frequencies in response to (i) a multiplexer and (ii) a configuration signal.

8. (TWICE AMENDED) The circuit according to claim 7, wherein said one or more reference clock frequencies are generated internally to said [programmable] device.

9. (TWICE AMENDED) The circuit according to claim 7, wherein said one or more reference clock frequencies are generated externally to said [programmable] device.

10. (TWICE AMENDED) A device selected from [the] a group consisting of programmable logic devices (PLDs), complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs), comprising the [circuit] device of claim 12.

12. (TWICE AMENDED) A [programmable] device comprising:

a [first circuit capable of storing programmable information] programmable logic circuit configured to (i) generate one or more control signals and (ii) receive one or more clock signals; and

a [second] phase lock loop circuit configured to generate said one or more clock signals, [capable of providing a plurality of output clocks] each capable of oscillating at a different one of a plurality of frequencies, said [output clocks] clock signals generated in response to (i) a reference clock [frequency] and (ii) said one or more control signals, wherein said programmable logic circuit and said phase lock loop circuit are integrated on a single circuit [programming inputs].

15. (TWICE AMENDED) A method for providing an integrated programmable logic circuit [device] and a phase lock loop [clock generation] circuit comprising the steps of:

(a) [storing programmable] manipulating information to generate one or more control signals and receive one or more clock signals; and

(b) generating [a plurality of output clocks] said one or more clock signals with [a] said phase lock loop circuit [(PLL)], each of said [output clocks] one or more clock signals being:

(i) capable of oscillating at a different one of a plurality of frequencies, and

(ii) generated in response to a reference clock frequency and said one or more control signals [programming inputs].

13 ~~16~~. (TWICE AMENDED) [A] The method according to claim 12 ~~15~~, further comprising the step of:

(c) individually programming each of said [plurality of output clocks] one or more clock signals to one of a plurality of independent frequencies.

14 ~~17~~. (TWICE AMENDED) [A] The method according to claim 13 ~~16~~, further comprising the step of:

(d) adjusting [the] an impedance of said [output clocks in response to said one or more programming inputs] one or more clock signals to match [the] an external impedance [of an external device].

15 ~~18~~. (TWICE AMENDED) [A] The method according to claim 13 [~~16~~] 15, further comprising the step of:

[(e)] (c) selecting said reference clock frequency from one or more [clocks] internal clock signals generated internally to said programmable logic circuit [device].

Sub D7 19. (TWICE AMENDED) [A] The method according to claim [16] 15, further comprising the step of:

[(e)] (c) selecting said reference clock frequency from one or more [clocks] external clock signals generated externally to said programmable circuit [device].

20. (TWICE AMENDED) [A] The method according to claim 16, further comprising the step of:

(d) selecting said reference clock frequency from one or more [clocks] second clock signals generated internally or externally to said programmable logic circuit [device].

Please add the following new claims:

21. (ADDED) The device according to claim 12, wherein said programmable logic circuit is further configured to generate one or more output signals in response to (i) one or more input signals and (ii) said one or more clock signals.

22. (ADDED) A device comprising:

means for manipulating information to generate one or more control signals, wherein said means for configuring receives one or more clock signals; and

means for generating said one or more clock signals in response to (i) a reference clock and (ii) said one or more control signals, wherein said one or more clock signals are each capable of oscillating at a different one of a plurality of frequencies, said

means for manipulating and said means for generating are integrated on a single circuit.

19. (ADDED) The device according to claim 18, wherein said one or more clock signals are individually programmable to oscillate at one of said plurality of frequencies.

24. (ADDED) The device according to claim 23, wherein said one or more clock signals each have an impedance that can be adjusted to match an impedance of an external device.

REMARKS

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a device comprising a programmable logic circuit and a phase lock loop circuit. The programmable logic circuit may manipulate information to generate one or more control signals and receive one or more clock signals. The phase lock loop circuit may be configured to generate the one or more clock signals, each capable of oscillating at a different one of a plurality of frequencies. The one or more clock signals may be generated in response to a reference clock frequency and the one or more control signals. The programmable logic circuit and the phase lock loop circuit may be integrated on a single circuit.